

July 1997 Revised March 1999

74VHCT00A Quad 2-Input NAND Gate

General Description

The VHCT00A is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC}=0$ V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to

5V systems and two supply systems such as battery backup.

Features

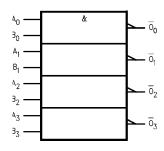
- High speed: $t_{PD} = 5.0$ ns (typ) at $T_A = 25$ °C
- High noise immunity: $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Power down protection is provided on all inputs and
- Low noise: V_{OLP} = 0.8V (max)
- Low power dissipation: $I_{CC} = 2 \mu A \text{ (max) at } T_A = 25^{\circ} C$
- Pin and function compatible with 74HCT00

Ordering Code:

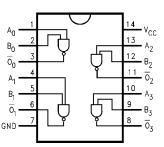
Order Number	Package Number	Package Description						
74VHCT00AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow						
74VHCT00ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide						
74VHCT00AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide						
74VHCT00AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide						

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description				
A _n , B _n	Inputs				
\overline{O}_n	Outputs				

Truth Table

Α	В	ō
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

Absolute Maximum Ratings(Note 1)

 $\begin{tabular}{lll} Supply Voltage (V_{CC}) & -0.5V to +7.0V \\ DC Input Voltage (V_{IN}) & -0.5V to +7.0V \\ \end{tabular}$

DC Output Voltage (V_{OUT})

 $\begin{array}{ll} \mbox{(Note 2)} & -0.5\mbox{V to V}_{CC} + 0.5\mbox{V} \\ \mbox{(Note 3)} & -0.5\mbox{V to 7.0\mbox{V}} \\ \mbox{Input Diode Current (I_{IK})} & -20\mbox{ mA} \end{array}$

Output Diode Current (I_{OK})

 $\begin{array}{ll} \mbox{(Note 4)} & \pm 20 \mbox{ mA} \\ \mbox{DC Output Current ($I_{\rm OUT}$)} & \pm 25 \mbox{ mA} \\ \mbox{DC V}_{\rm CC}/\mbox{GND Current ($I_{\rm CC}$)} & \pm 50 \mbox{ mA} \\ \mbox{Storage Temperature ($T_{\rm STG}$)} & -65\mbox{°C to } +150\mbox{°C} \\ \end{array}$

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 5)

Supply Voltage (V_{CC}) 4.5V to 5.5V Input Voltage (V_{IN}) 0V to +5.5V

 $\begin{aligned} & \text{Input Voltage (V}_{\text{IN}}) \\ & \text{Output Voltage (V}_{\text{OUT}}) \end{aligned}$

(Note 2) 0V to V_{CC} (Note 3) 0V to 5.5V Operating Temperature (T_{OPR}) $-40^{\circ}C$ to $+85^{\circ}C$

Operating Temperature (T_{OPR}) Input Rise and Fall Time (t_r, t_f)

 $V_{CC} = 5.0 \text{V} \pm 0.5 \text{V}$ 0 ns/V ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifica-

Note 2: HIGH or LOW state. I_{OUT} absolute maximum rating must be

observed.

Note 3: $V_{CC} = 0V$.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ (Outputs Active)

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	v _{cc}	T _A = 25°C			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
Cynnbon	i arameter	(V)	Min	Тур	Max	Min	Max	Oiiita	Conditions	
V _{IH}	HIGH Level Input Voltage	4.5	2.0			2.0		V		
		5.5	2.0			2.0		· ·		
V _{IL}	LOW Level Input Voltage	4.5			0.8		0.8	V		
		5.5			0.8		0.8	V		
V _{OH}	HIGH Level Output Voltage	4.5	4.40	4.50		4.40		V	$V_{IN} = V_{IH}$	$I_{OH} = -50 \mu A$
		4.5	3.94			3.80		V	or V _{IL}	$I_{OH} = -8 \text{ mA}$
V _{OL}	LOW Level Output Voltage	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$	$I_{OL} = 50 \mu A$
		4.5			0.36		0.44	V	or V _{IL}	$I_{OL} = 8 \text{ mA}$
I _{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	μΑ	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5			2.0		20.0	μΑ	V _{IN} = V _{CC} or GND	
I _{CCT}	Maximum I _{CC} / Input	5.5			1.35		1.50	mA	$V_{IN} = 3.4V$ Other Inputs = V_{CC} or GND	
I _{OFF}	Output Leakage Current	0.0			0.5		5.0	μΑ	V _{OUT} = 5.5V	
	(Power Down State)									

Noise Characteristics

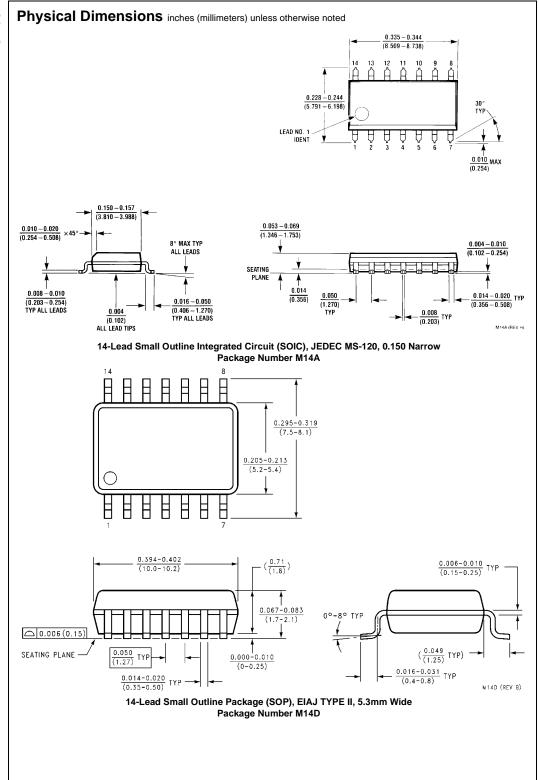
Symbol	Parameter	V _{CC} (V)	T _A =	25°C	Units	Conditions	
- Cyllibol	T drameter		Тур	Limit	Omio		
V _{OLP} (Note 6)	Quiet Output Maximum Dynamic V _{OL}	5.0	0.4	0.8	V	C _L = 50 pF	
V _{OLV} (Note 6)	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.4	-0.8	V	C _L = 50 pF	
V _{IHD} (Note 6)	Minimum HIGH Level Dynamic Input Voltage	5.0		2.0	V	C _L = 50 pF	
V _{ILD} (Note 6)	Maximum LOW Level Dynamic Input Voltage	5.0		0.8	V	C _L = 50 pF	

Note 6: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	$T_A = 25^{\circ}C$			T _A = -40°	C to +85°C	Units	Conditions
- Cyllibol			Min	Тур	Max	Min	Max	Oilles	Conditions
t _{PLH}	Propagation Delay	5.0 ± 0.5		5.0	6.9	1.0	8.0	ns	C _L = 15 pF
t _{PHL}				5.5	7.9	1.0	9.0	115	C _L = 50 pF
C _{IN}	Input Capacitance			4	10		10	pF	V _{CC} = Open
C _{PD}	Power Dissipation Capacitance			17				pF	(Note 7)

Note 7: C_{PD} is defined as the value of the internal equivalent capacitance, which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per gate)



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 0.43 TYP -A-7.72 4.16 6.4 4.4±0.1 -B-3.2 ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT. SEE DETAIL A ALL LEAD TIPS 0.90+0.15 1.2 MAX [0.09-0.20 -C-L_{0.10±0.05} 0.65 412.00°ТОР & ВОТТОМ R0.16 R0.31-GAGE PLANE NDTES: 0.25 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ABJREF NOTE 6, DATED 7/930°-8° B. DIMENSIONS ARE IN MILLIMETERS C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS 0.6±0.1 SEATING PLANE -1.00-DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 (1.524) 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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8.255 + 1.016

N14A (REV F)

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